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## (54) Computer system with derived local bus

(57) An integrated processor is provided that includes a CPU core, a local bus coupled to the CPU core, and a variety of peripheral such as a memory controller, a direct memory access controller, and an interrupt controller coupled to the local bus. A bus interface unit is further provided to interface between the CPU local bus and a PCI standard multiplexed peripheral bus. The CPU core, the memory controller, the direct memory access controller, the interrupt controller, and the bus interface unit are all incorporated on a common integrated circuit chip. A local bus control unit is further provided that is capable of generating a loading signal and an address strobe signal synchronously with certain bus cy-

cles that are executed on the PCI bus. The local bus control unit allows external peripheral devices that are compatible with the CPU local bus protocols to be connected through the PCI bus. A latch is coupled to the multiplexed address/data (A/D) lines of the PCI bus and includes a set of output lines coupled to the address input lines of the externally connected peripheral device. The external latch is latched by the loading signal. The cycle definition signals of the PCI bus are further latched within the external latch to provide memory/I/O and read/write signals to the external peripheral device. The data lines of the peripheral device may be connected directly to the multiplexed address/data lines of the PCI bus.

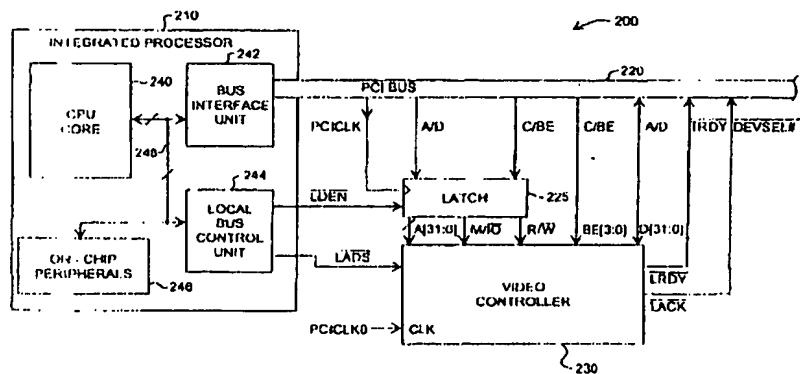


FIG. 2



## EUROPEAN SEARCH REPORT

Application Number

EP 94 30 9252

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Reference of document with indication, where applicable, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl 6)
A	US 5 175 084 A (BEGIN RALPH M ET AL) * column 1, line 23 - column 2, line 7 * * column 2, line 59 - column 3, line 44 * * column 4, line 38 - column 5, line 23 * * abstract: claims 1-3; figures 2,7 * -----	1,3,5,6 12-18	G06F 13/42
A	US 5 253 353 A (MOGUL JEFFREY C) * column 2, line 23 - line 60 * * column 3, line 13 - column 4, line 46 * * abstract, claims 1,2; figure 1 *	1-20	
A	US 5 005 121 A (NAKADA KUNIHIKO ET AL) * column 2, line 41 - column 3, line 65 * * abstract *	1,12,15 -----	

TECHNICAL FIELDS  
SEARCHED (Int.Cl 6)

G06F

The present search report has been drawn up for all claims

Date of search	Date of completion of the search	Examiner
THE HAGUE	27 January 1998	Nguyen Xuan Hiep, C
CATEGORIES OF CITED DOCUMENTS		
<input checked="" type="checkbox"/> A particularly relevant taken alone <input checked="" type="checkbox"/> B particularly relevant if combined with another document of the same category <input type="checkbox"/> C Technological background <input type="checkbox"/> D Prior written disclosure <input type="checkbox"/> E Intermediary document		
<input type="checkbox"/> F Theory or principle underlying the invention <input type="checkbox"/> G Earlier patent document, but published after the filing date <input type="checkbox"/> H Document cited in the application <input type="checkbox"/> I Document cited for other reasons <input type="checkbox"/> J Member of the same patent family, corresponding document		

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